

Fig. 1 (Prior Art)

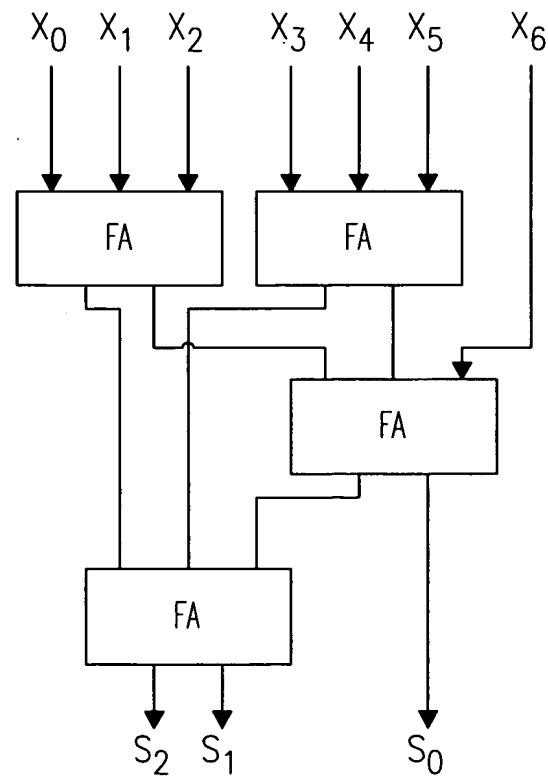


Fig. 2 (Prior Art)

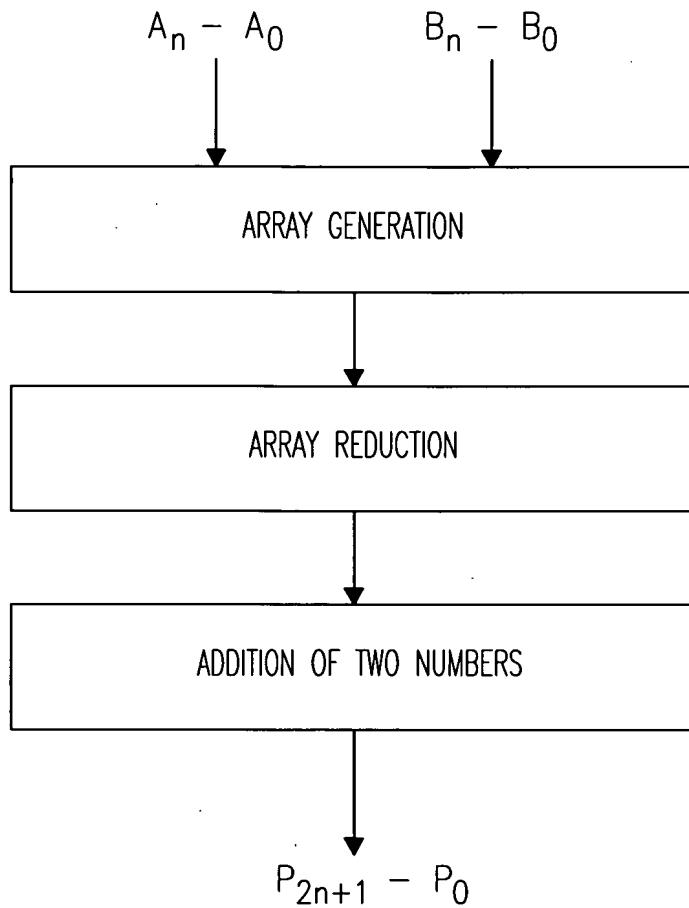
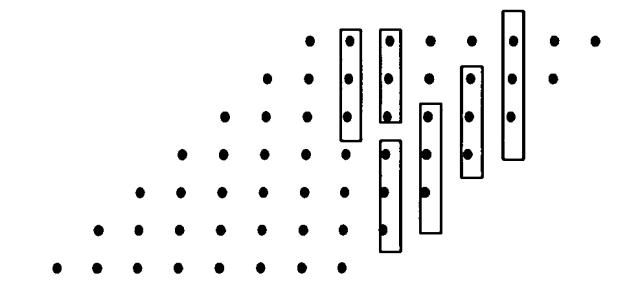
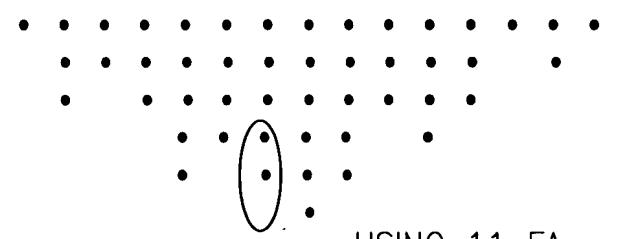


Fig. 3 (Prior Art)

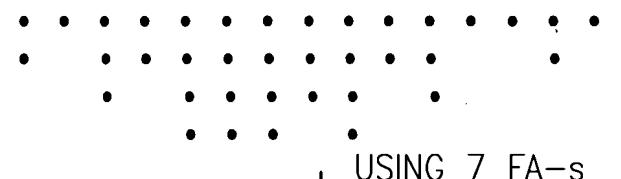
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	A ₇ B ₁	A ₆ B ₁	A ₅ B ₁	A ₄ B ₁	A ₃ B ₁	A ₂ B ₁	A ₁ B ₁	A ₀ B ₁
	A ₇ B ₂	A ₆ B ₂	A ₅ B ₂	A ₄ B ₂	A ₃ B ₂	A ₂ B ₂	A ₁ B ₂	A ₀ B ₂
	A ₇ B ₃	A ₆ B ₃	A ₅ B ₃	A ₄ B ₃	A ₃ B ₃	A ₂ B ₃	A ₁ B ₃	A ₀ B ₃
	A ₇ B ₄	A ₆ B ₄	A ₅ B ₄	A ₄ B ₄	A ₃ B ₄	A ₂ B ₄	A ₁ B ₄	A ₀ B ₄
	A ₇ B ₅	A ₆ B ₅	A ₅ B ₅	A ₄ B ₅	A ₃ B ₅	A ₂ B ₅	A ₁ B ₅	A ₀ B ₅
	A ₇ B ₆	A ₆ B ₆	A ₅ B ₆	A ₄ B ₆	A ₃ B ₆	A ₂ B ₆	A ₁ B ₆	A ₀ B ₆
	A ₇ B ₇	A ₆ B ₇	A ₅ B ₇	A ₄ B ₇	A ₃ B ₇	A ₂ B ₇	A ₁ B ₇	A ₀ B ₇



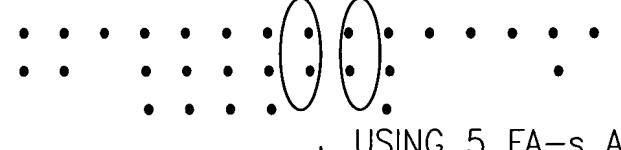
USING 16 FA BLOCKS



USING 11 FA-s AND 1 HA



USING 7 FA-s



USING 5 FA-s AND 2 HA-s

Fig. 4 (Prior Art)

TITLE: MULTIPLICATION LOGIC CIRCUIT
INVENTORS NAME: Sunil Talwar et al.
DOCKET NO.: 1365.048US1

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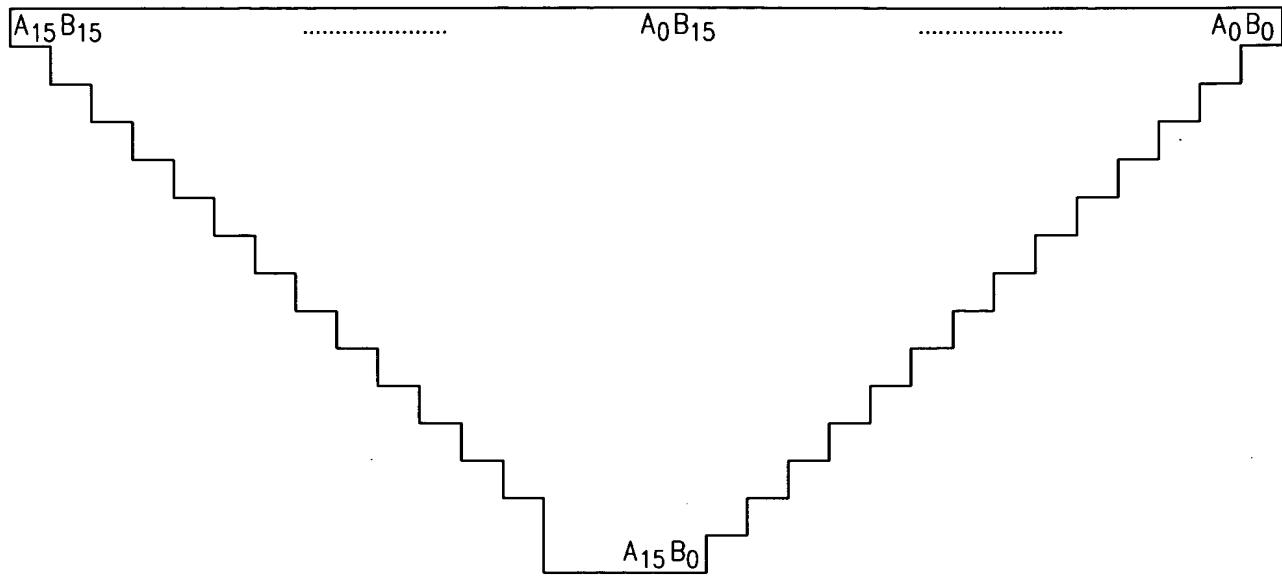


Fig. 5

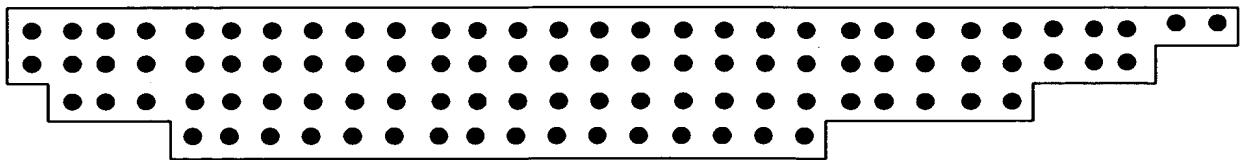


Fig. 6

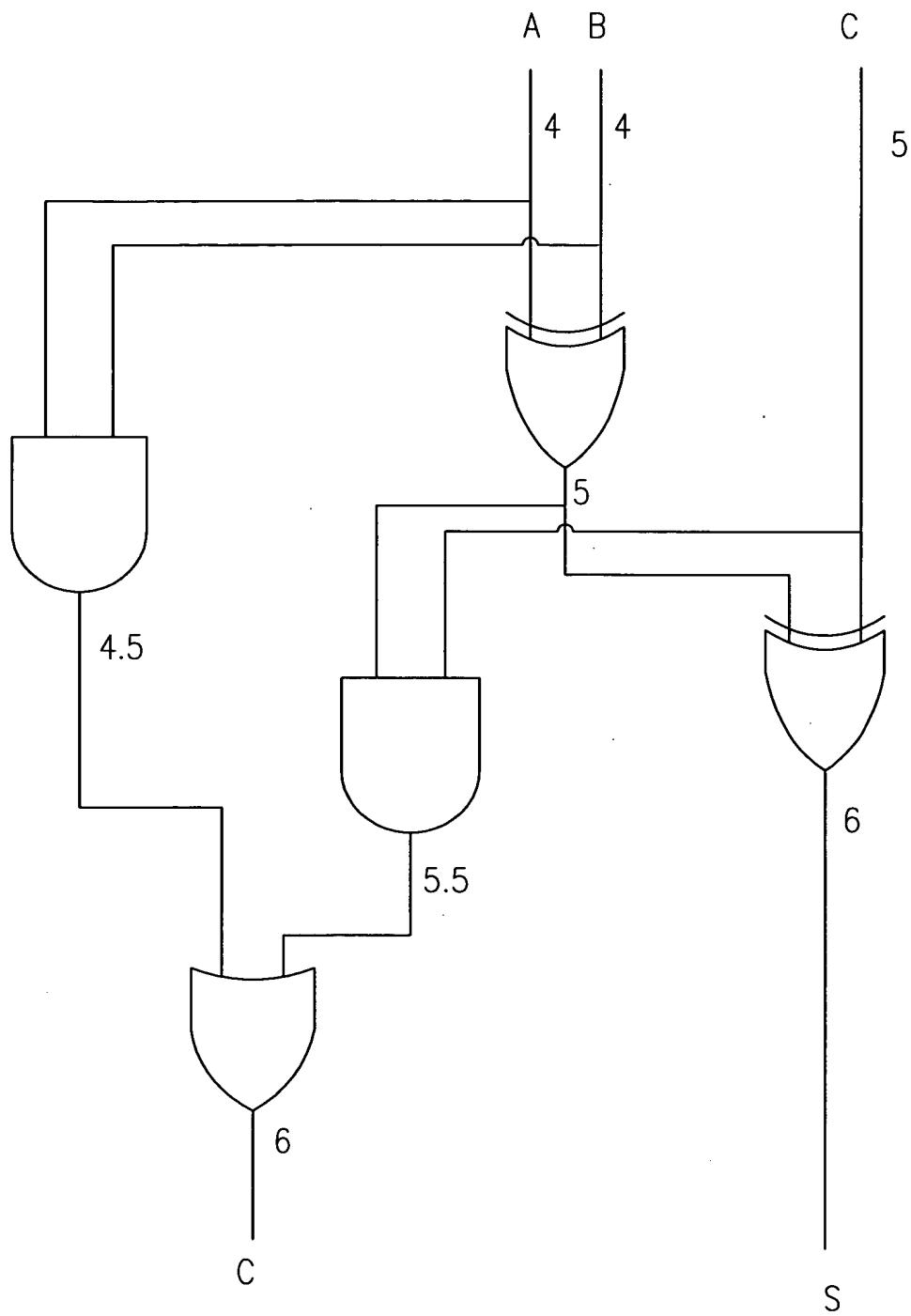


Fig. 7

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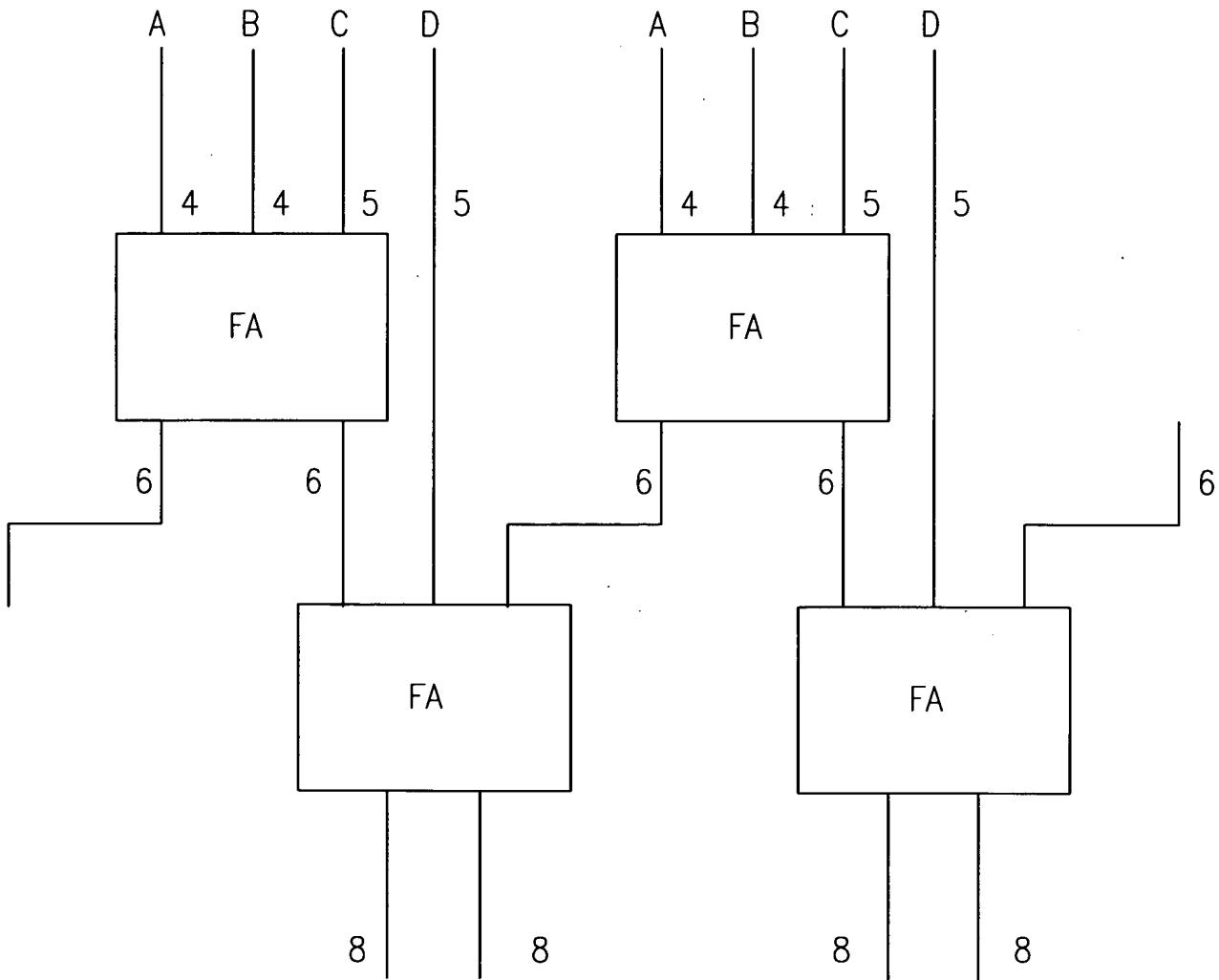


Fig.8

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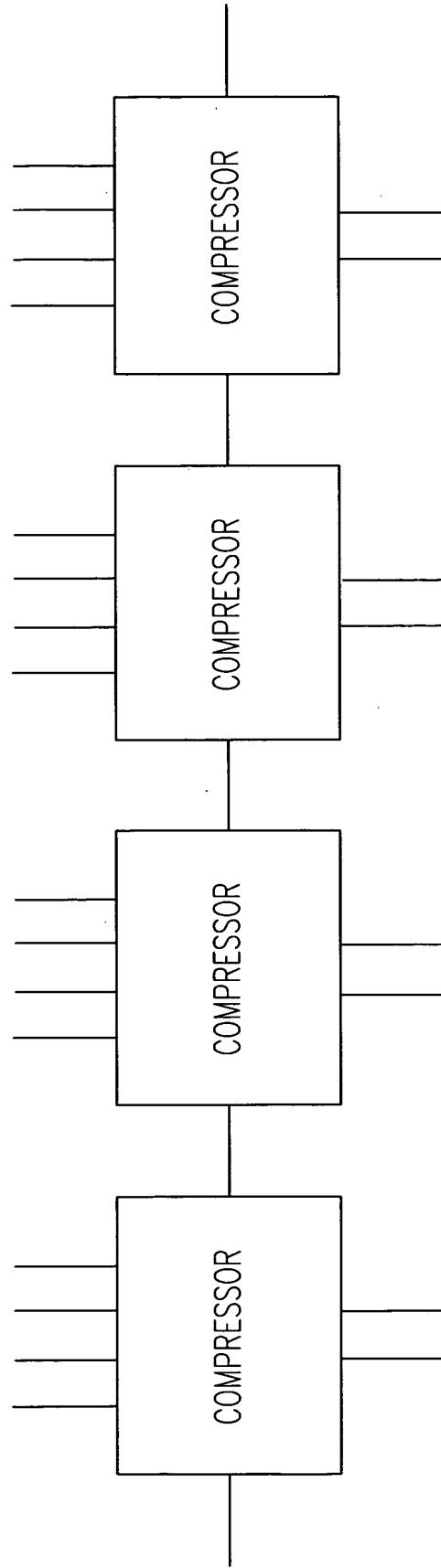


Fig. 9

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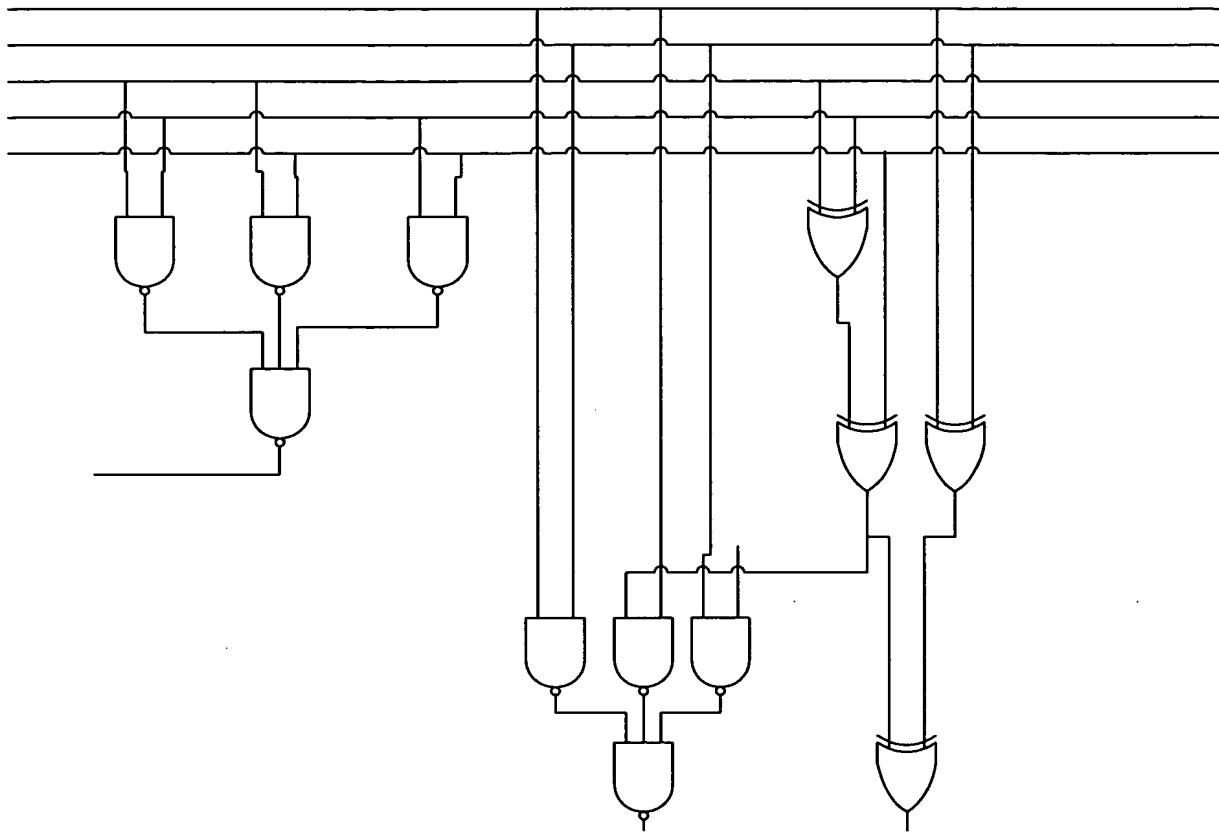


Fig. 10